FIG. 1

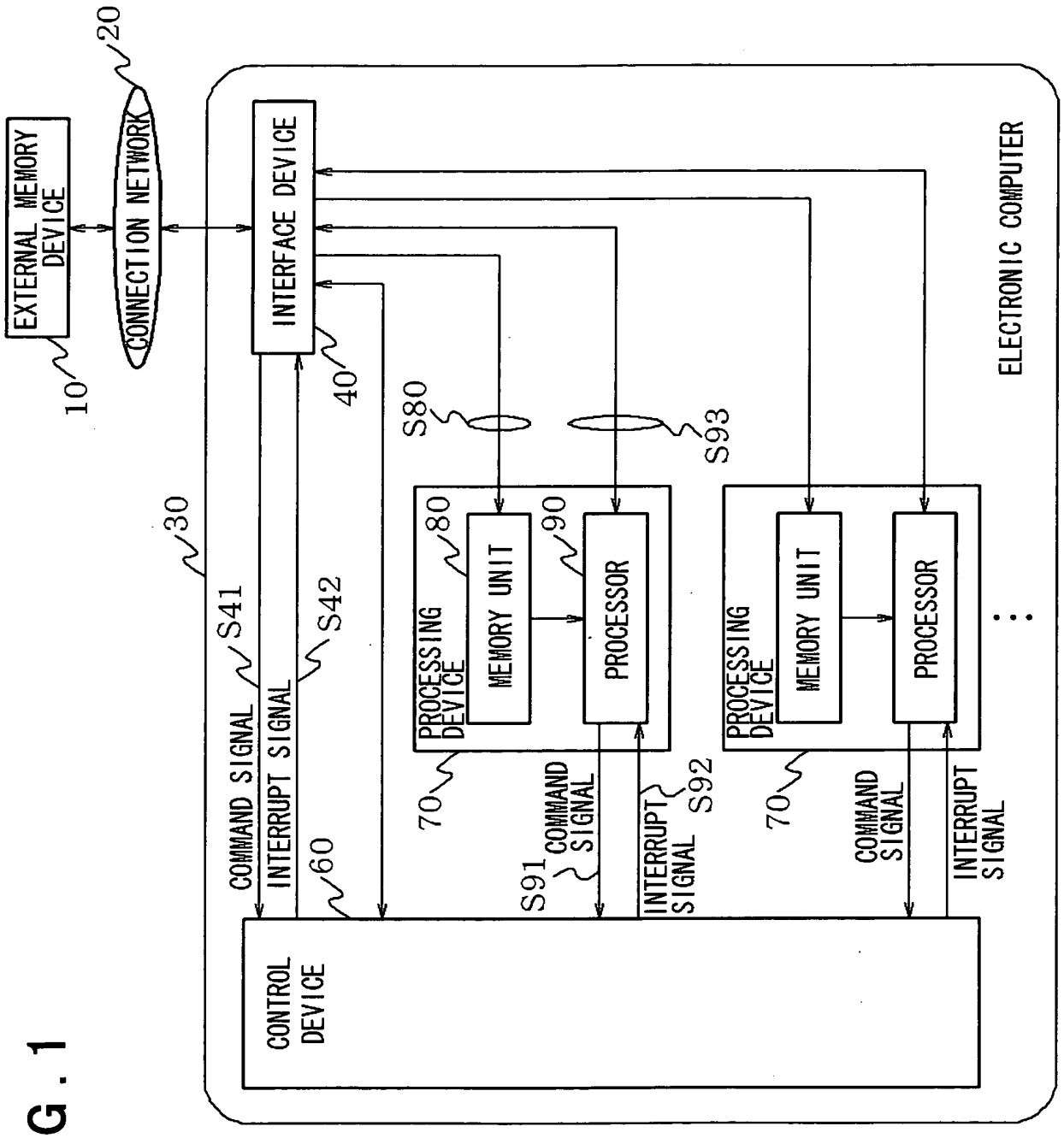
EXTERNAL MEMORY DEVICE
10
CONNECTION NETWORK
20
INTERFACE DEVICE
40
ELECTRONIC COMPUTER
30
S80
S93
PROCESSING DEVICE
80
MEMORY UNIT
90
PROCESSOR
70
COMMAND SIGNAL
INTERRUPT SIGNAL
S41
S42
S91
S92
60
CONTROL DEVICE

FIG . 2

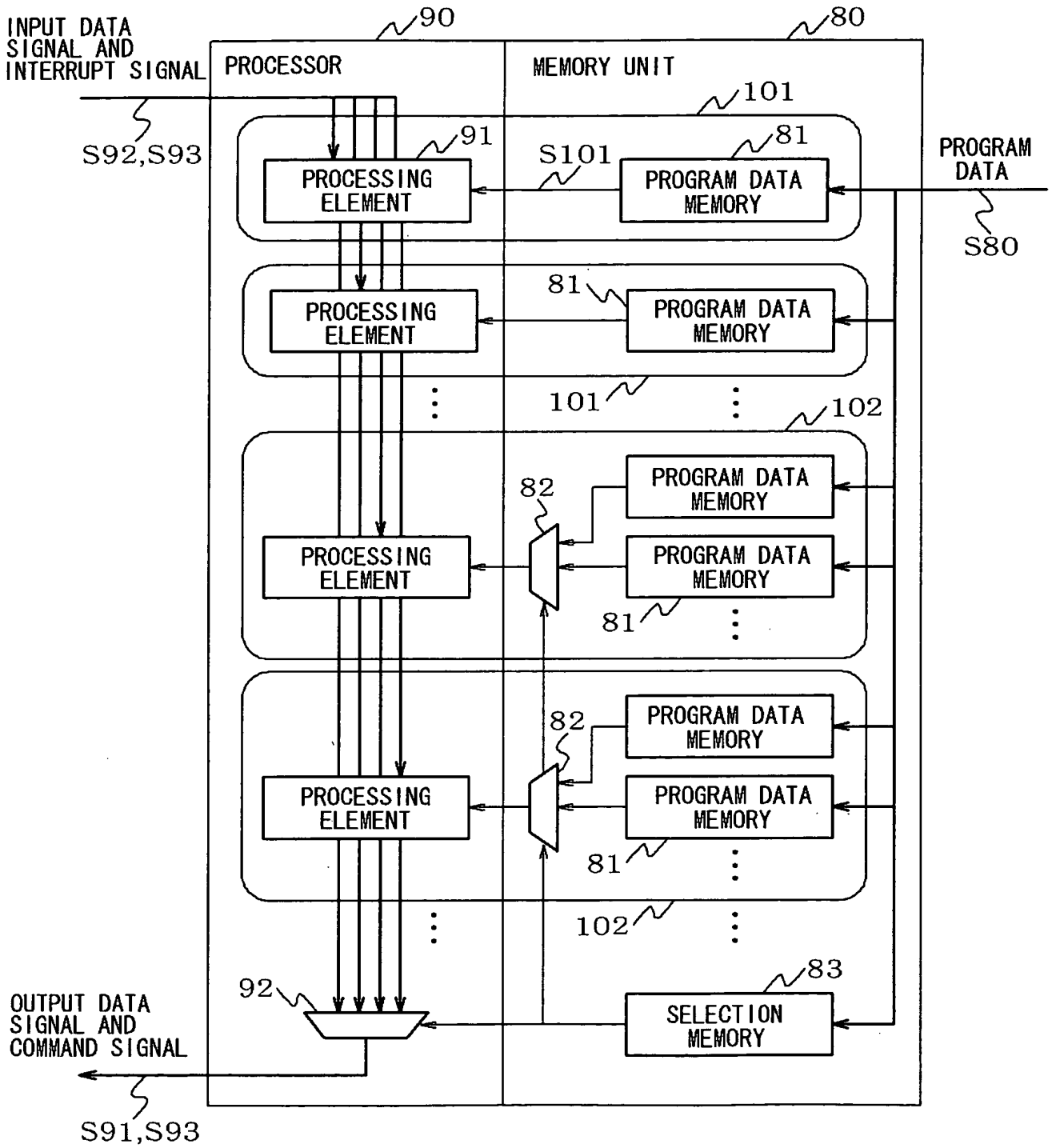
INPUT DATA SIGNAL AND INTERRUPT SIGNAL
S92,S93
90
PROCESSOR
80
MEMORY UNIT
101
91
PROCESSING ELEMENT
S101
81
PROGRAM DATA MEMORY
PROGRAM DATA
S80
102
82
92
83
SELECTION MEMORY
OUTPUT DATA SIGNAL AND COMMAND SIGNAL
S91,S93

FIG . 3

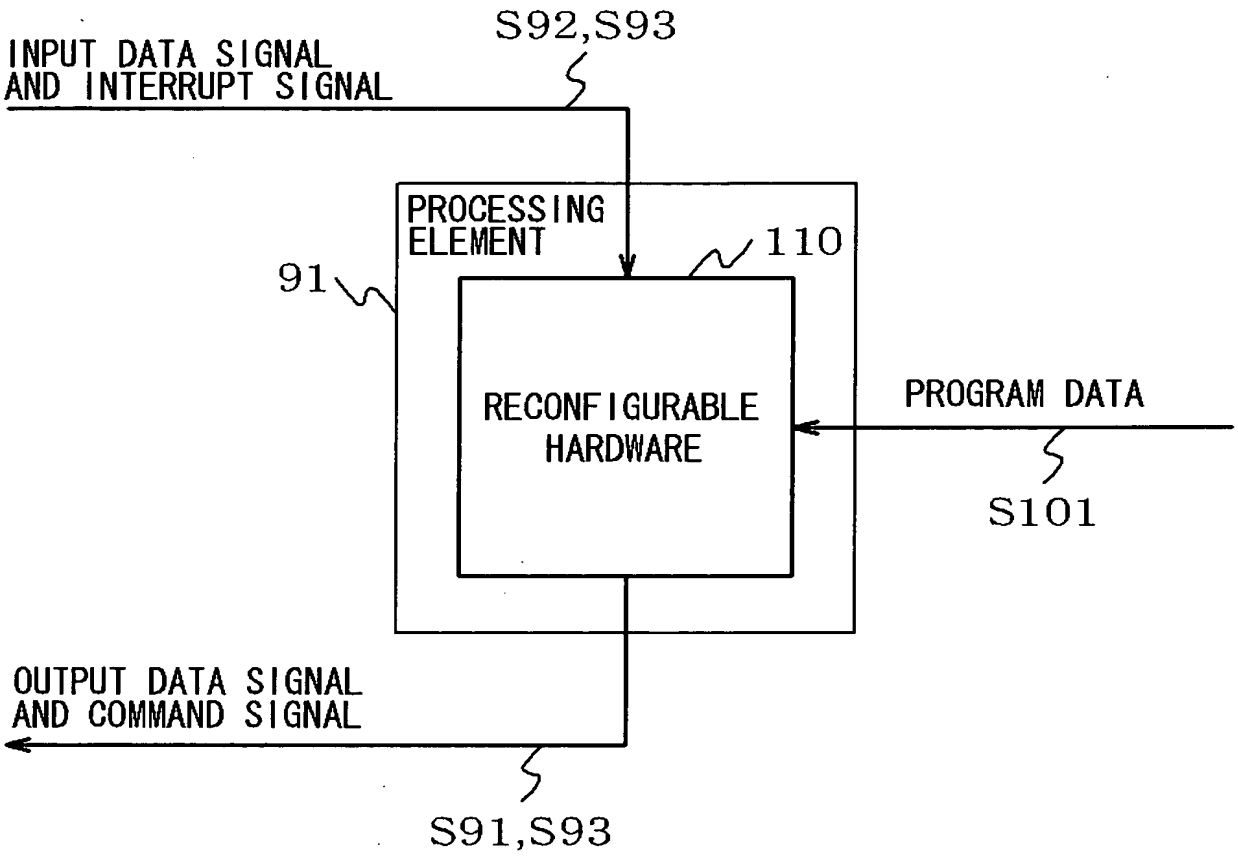
S92,S93
INPUT DATA SIGNAL
AND INTERRUPT SIGNAL
PROCESSING
ELEMENT
110
91
RECONFIGURABLE
HARDWARE
PROGRAM DATA
S101
OUTPUT DATA SIGNAL
AND COMMAND SIGNAL
S91,S93

FIG . 4

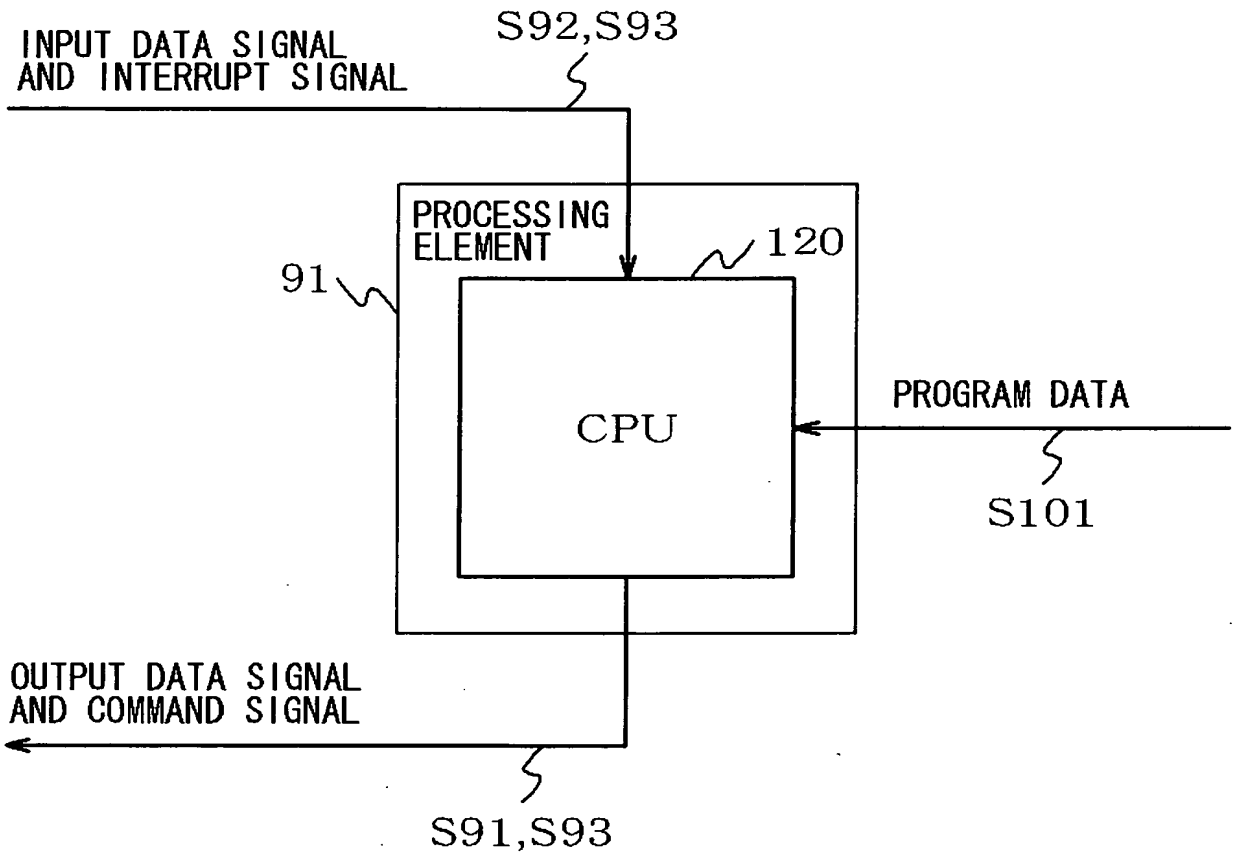
INPUT DATA SIGNAL
AND INTERRUPT SIGNAL
S92,S93
PROCESSING
ELEMENT
120
91
CPU
PROGRAM DATA
S101
OUTPUT DATA SIGNAL
AND COMMAND SIGNAL
S91,S93

FIG. 5

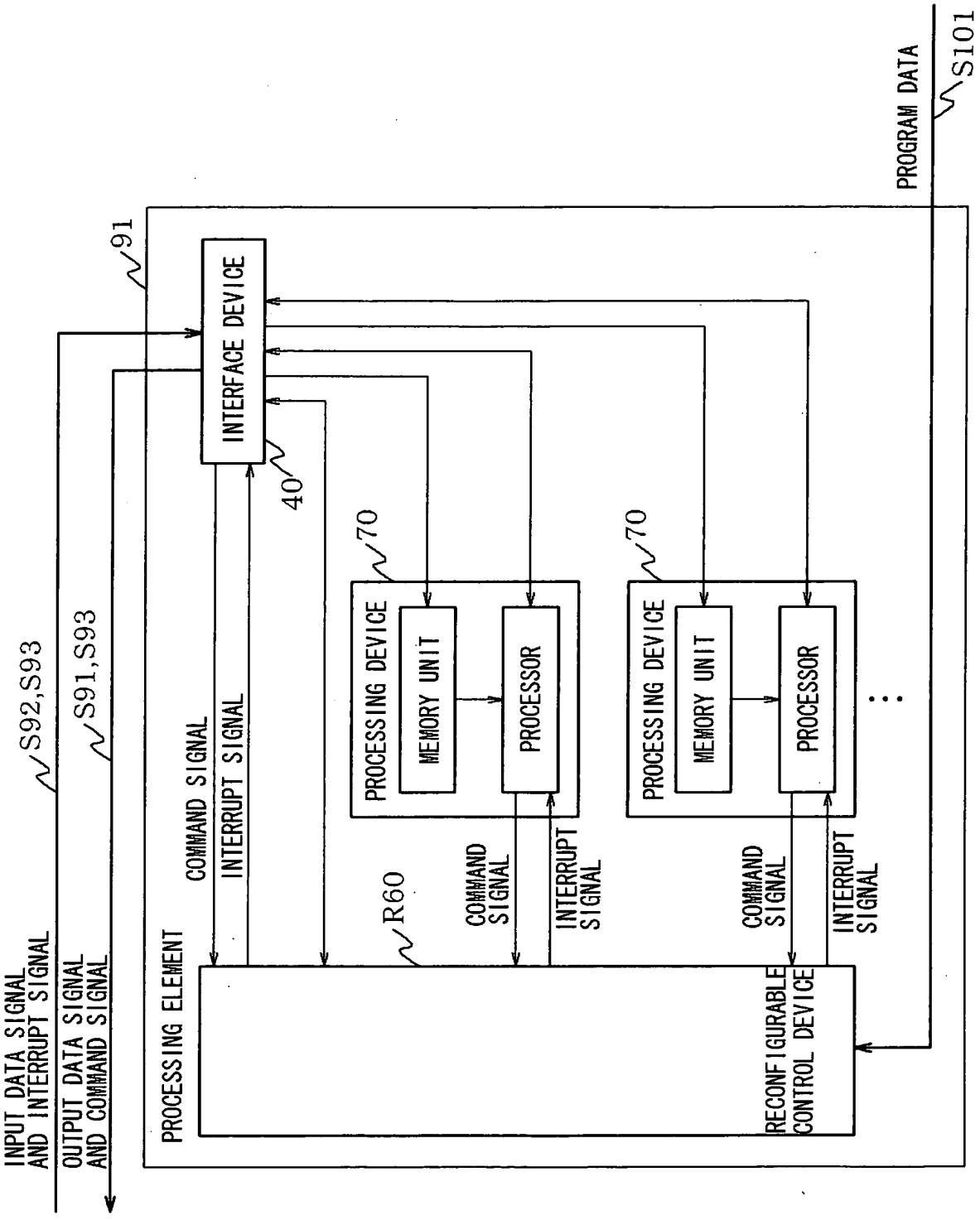
INPUT DATA SIGNAL AND INTERRUPT SIGNAL
OUTPUT DATA SIGNAL AND COMMAND SIGNAL
S92,S93
S91,S93
91
INTERFACE DEVICE
40
PROGRAM DATA
S101
PROCESSING ELEMENT
COMMAND SIGNAL
INTERRUPT SIGNAL
R60
70
PROCESSING DEVICE
MEMORY UNIT
PROCESSOR
RECONFIGURABLE CONTROL DEVICE

FIG. 6

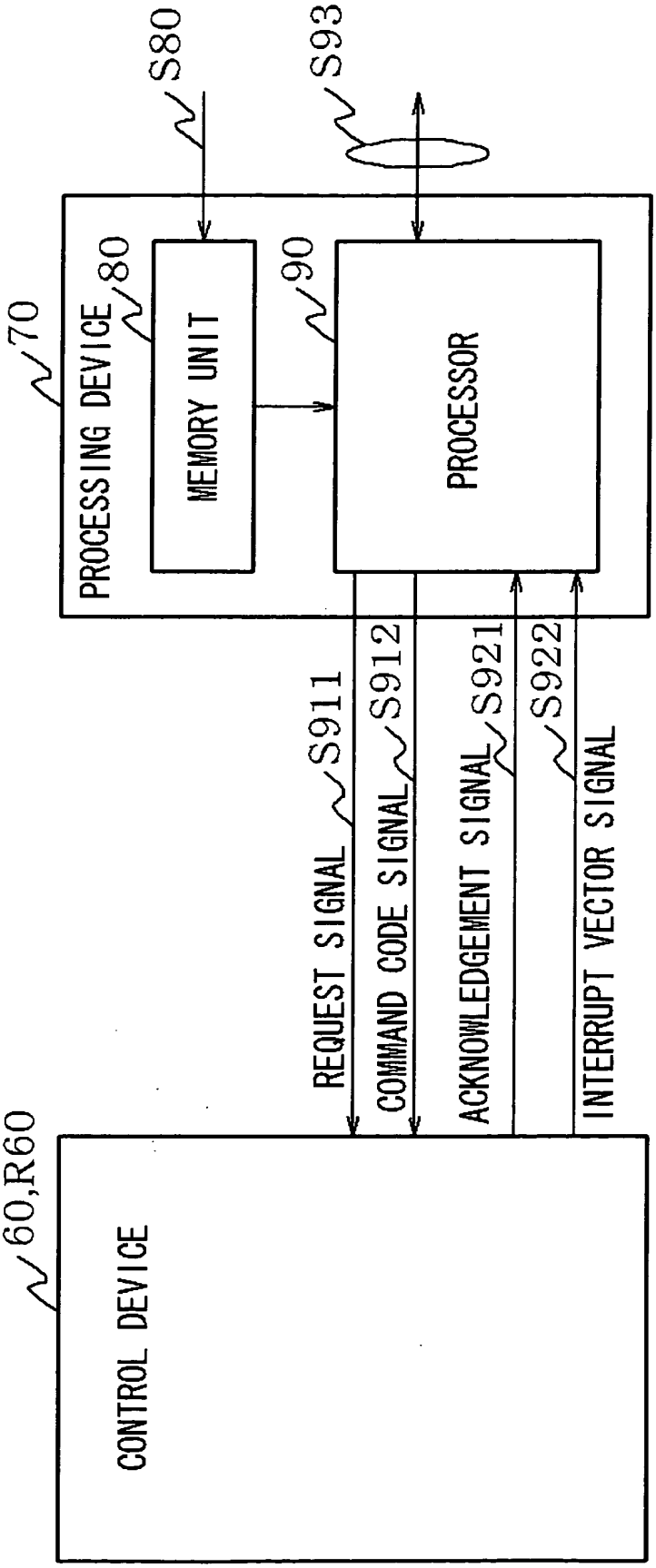
S80
S93
70
PROCESSING DEVICE
80
MEMORY UNIT
90
PROCESSOR
S911
REQUEST SIGNAL
S912
COMMAND CODE SIGNAL
S921
ACKNOWLEDGEMENT SIGNAL
S922
INTERRUPT VECTOR SIGNAL
60,R60
CONTROL DEVICE

FIG . 7

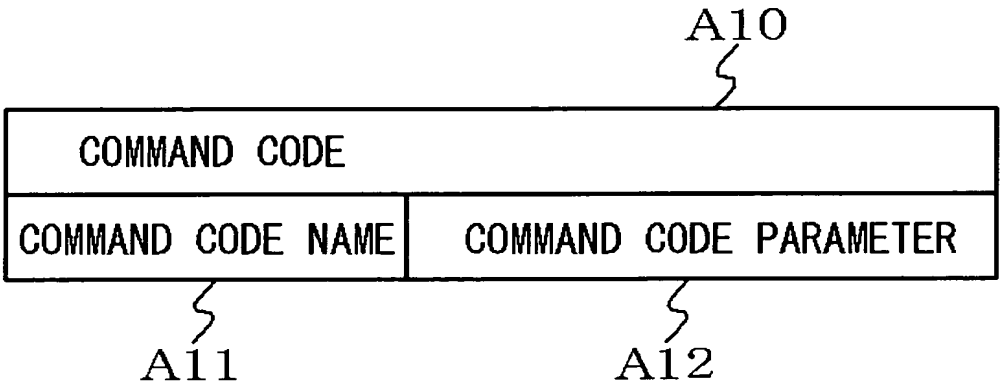
A10
COMMAND CODE
COMMAND CODE NAME
COMMAND CODE PARAMETER
A11
A12

FIG . 8

COMMAND CODE NAME	COMMAND CODE PARAMETER	CONTENTS
activate	PROCESSING ELEMENT	SELECTS A SPECIFIED PROCESSING ELEMENT, STARTS A OPERATION
halt	PROCESSING DEVICE	HALTS A OPERATION OF A SPECIFIED PROCESSING DEVICE
lnterrupt	PROCESSING DEVICE AND INTERRUPT VECTOR NUMBER	ISSUES A SPECIFIED INTERRUPT VECTOR NUMBER TO A SPECIFIED PROCESSING DEVICE
load_prg	REGION OF PROGRAM DATA MEMORY AND MEMORY REGION WHERE PROGRAM DATA IS STORED	TRANSFERS A PROGRAM DATA STORED IN A SPECIFIED MEMORY REGION TO A REGION OF A SPECIFIED PROGRAM DATA MEMORY
cancel_prg	REGION OF PROGRAM DATA MEMORY AND MEMORY REGION WHERE PROGRAM DATA IS STORED	CANCELS A TRANSFER OF A PROGRAM DATA STORED IN A SPECIFIED MEMORY REGION TO A REGION OF A SPECIFIED PROGRAM DATA MEMORY
wait_prg	REGION OF PROGRAM DATA MEMORY AND MEMORY REGION WHERE PROGRAM DATA IS STORED	WAITS UNTIL A TRANSFER OF A PROGRAM DATA STORED IN A SPECIFIED MEMORY REGION TO A REGION OF A SPECIFIED PROGRAM DATA MEMORY IS COMPLETE

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Inventor(s): Takeshi INUO
DOCKET NO.: 029471-0194

FIG. 9

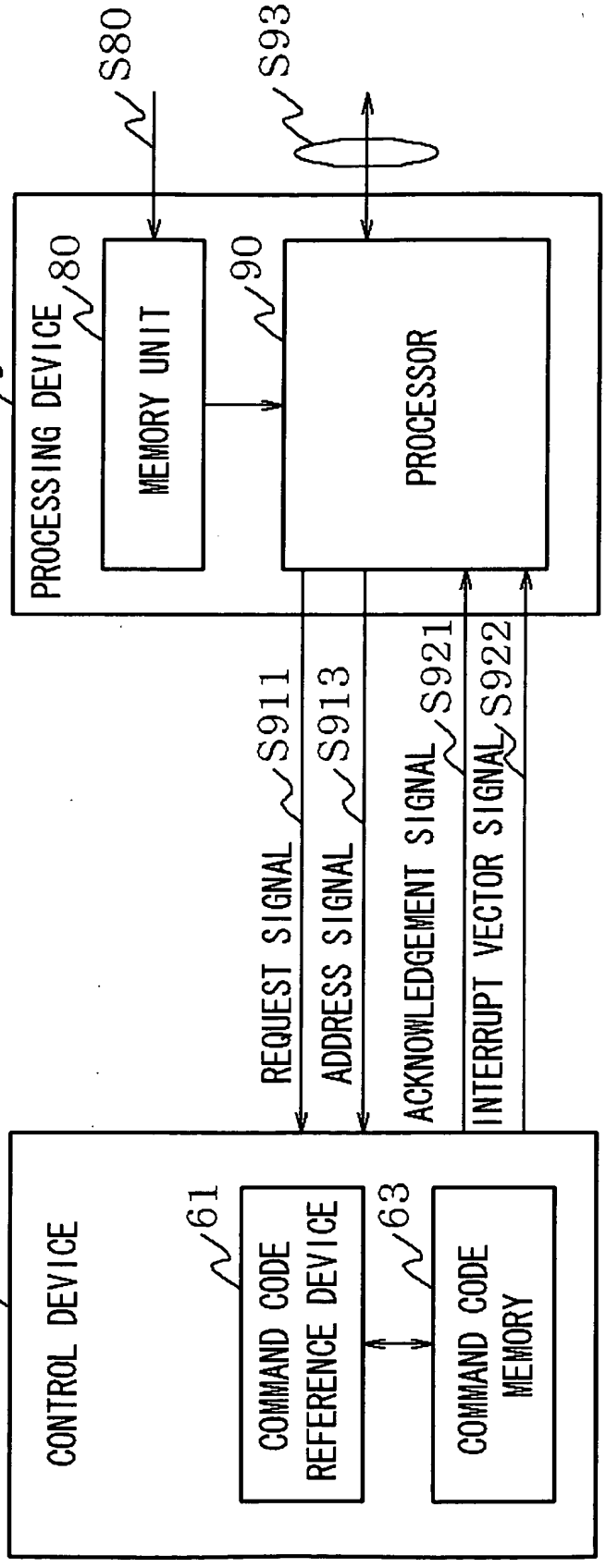
S80
S93
70
PROCESSING DEVICE
80
MEMORY UNIT
90
PROCESSOR
S911
REQUEST SIGNAL
S913
ADDRESS SIGNAL
S921
ACKNOWLEDGEMENT SIGNAL
S922
INTERRUPT VECTOR SIGNAL
60,R60
CONTROL DEVICE
61
COMMAND CODE REFERENCE DEVICE
63
COMMAND CODE MEMORY

FIG . 10

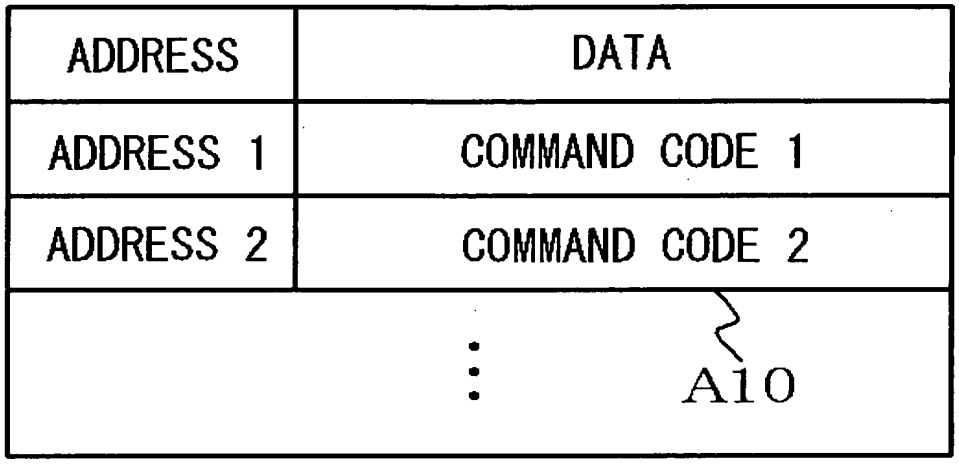
ADDRESS
DATA
ADDRESS 1
COMMAND CODE 1
ADDRESS 2
COMMAND CODE 2
A10

FIG. 11

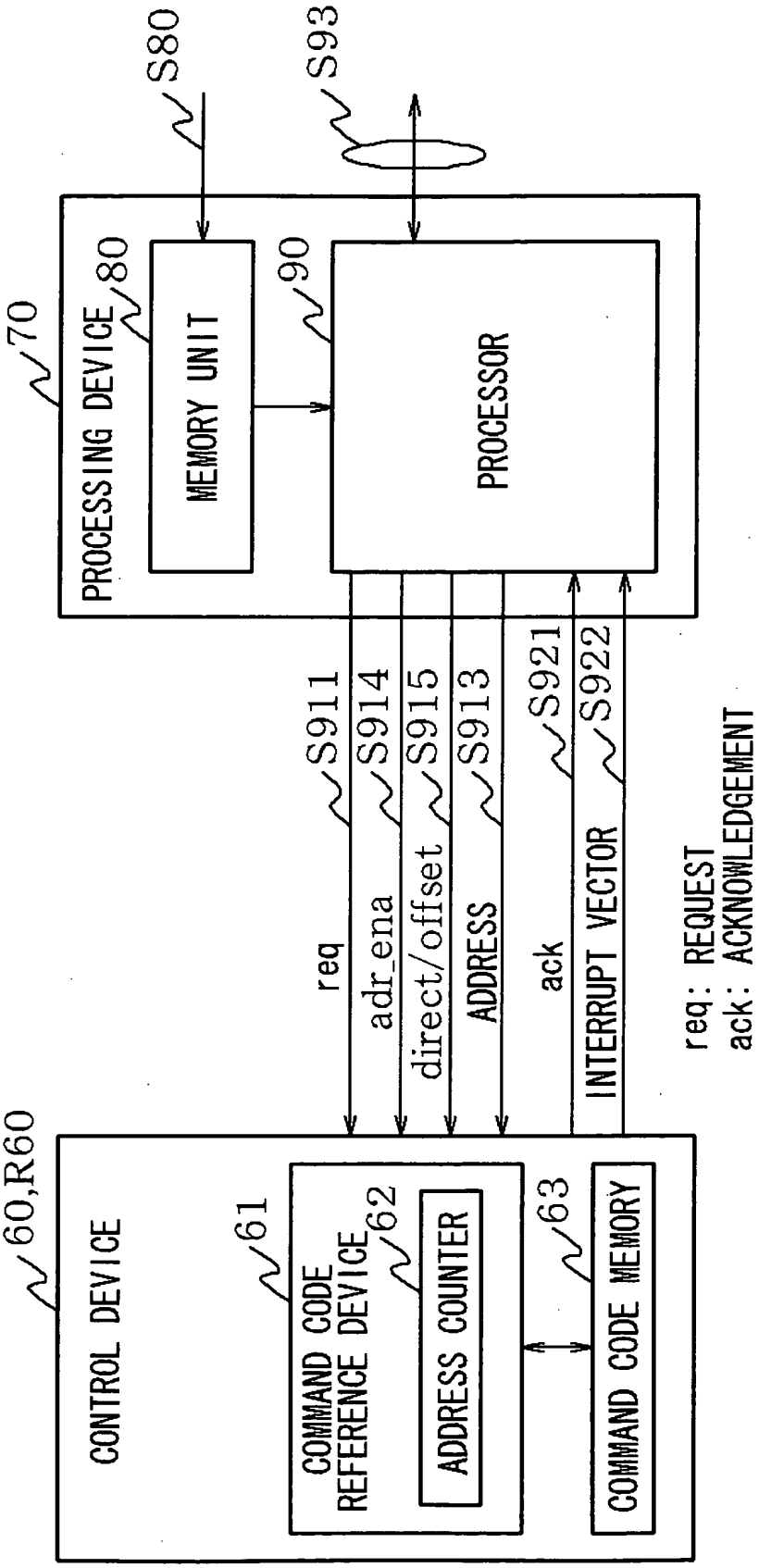
S80
S93
70
PROCESSING DEVICE
80
MEMORY UNIT
90
PROCESSOR
S911
S914
S915
S913
S921
S922
req
adr_ena
direct/offset
ADDRESS
ack
INTERRUPT VECTOR
req: REQUEST
ack: ACKNOWLEDGEMENT
60,R60
CONTROL DEVICE
61
COMMAND CODE
REFERENCE DEVICE
62
ADDRESS COUNTER
63
COMMAND CODE MEMORY

FIG . 12

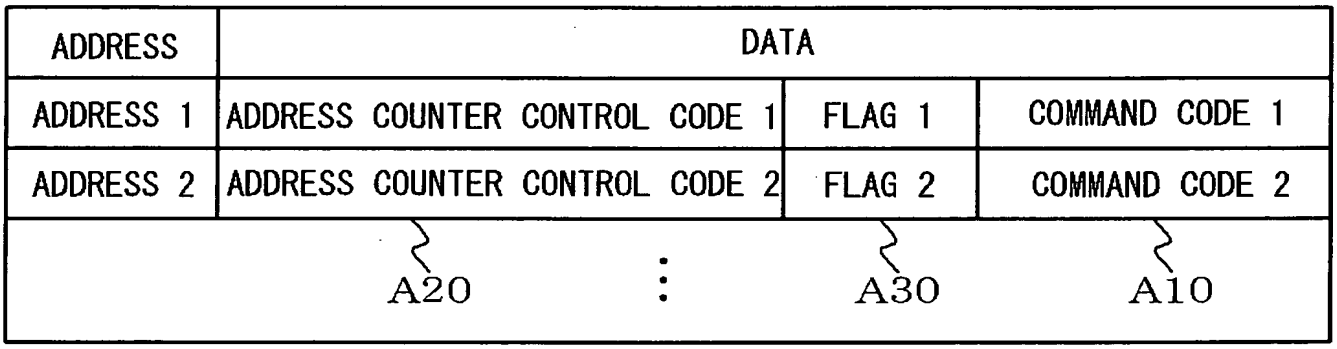
ADDRESS
DATA
ADDRESS 1
ADDRESS COUNTER CONTROL CODE 1
FLAG 1
COMMAND CODE 1
ADDRESS 2
ADDRESS COUNTER CONTROL CODE 2
FLAG 2
COMMAND CODE 2
A20
A30
A10

FIG . 13

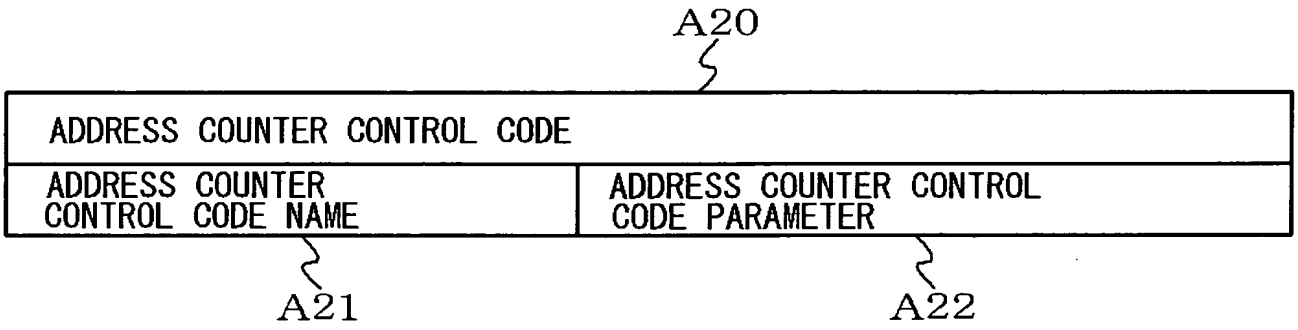
A20
ADDRESS COUNTER CONTROL CODE
ADDRESS COUNTER CONTROL CODE NAME
ADDRESS COUNTER CONTROL CODE PARAMETER
A21
A22

FIG .14

ADDRESS COUNTER CONTROL CODE NAME	ADDRESS COUNTER CONTROL CODE PARAMETER	CONTENTS
load_adr	N	SETS N AS THE VALUE OF THE ADDRESS COUNTER
add_adr	N	ADDS N TO THE VALUE OF THE ADDRESS COUNTER
push_adr	N	HIDES THE VALUE OF THE ADDRESS COUNTER IN THE ADDRESS COUNTER STACK AND SETS N AS A NEW VALUE
pop_adr		RETURNS THE VALUE OF THE ADDRESS COUNTER FROM THE ADDRESS COUNTER STACK

N: NUMERICAL VALUE

FIG .15

ADDRESS	DATA	
	ADDRESS COUNTER CONTROL CODE AND FLAG	COMMAND CODE
⋮	X100 ⋮	Y100
100	add_adr 1 | cont	COMMAND CODE 100
101	load_adr 200 | cont	COMMAND CODE 101
⋮	X101 ⋮ X200	Y101 Y200
200	add_adr 1 | stop	COMMAND CODE 100
201	ADDRESS COUNTER CONTROL CODE 201	COMMAND CODE 101
⋮	⋮	

FIG. 16

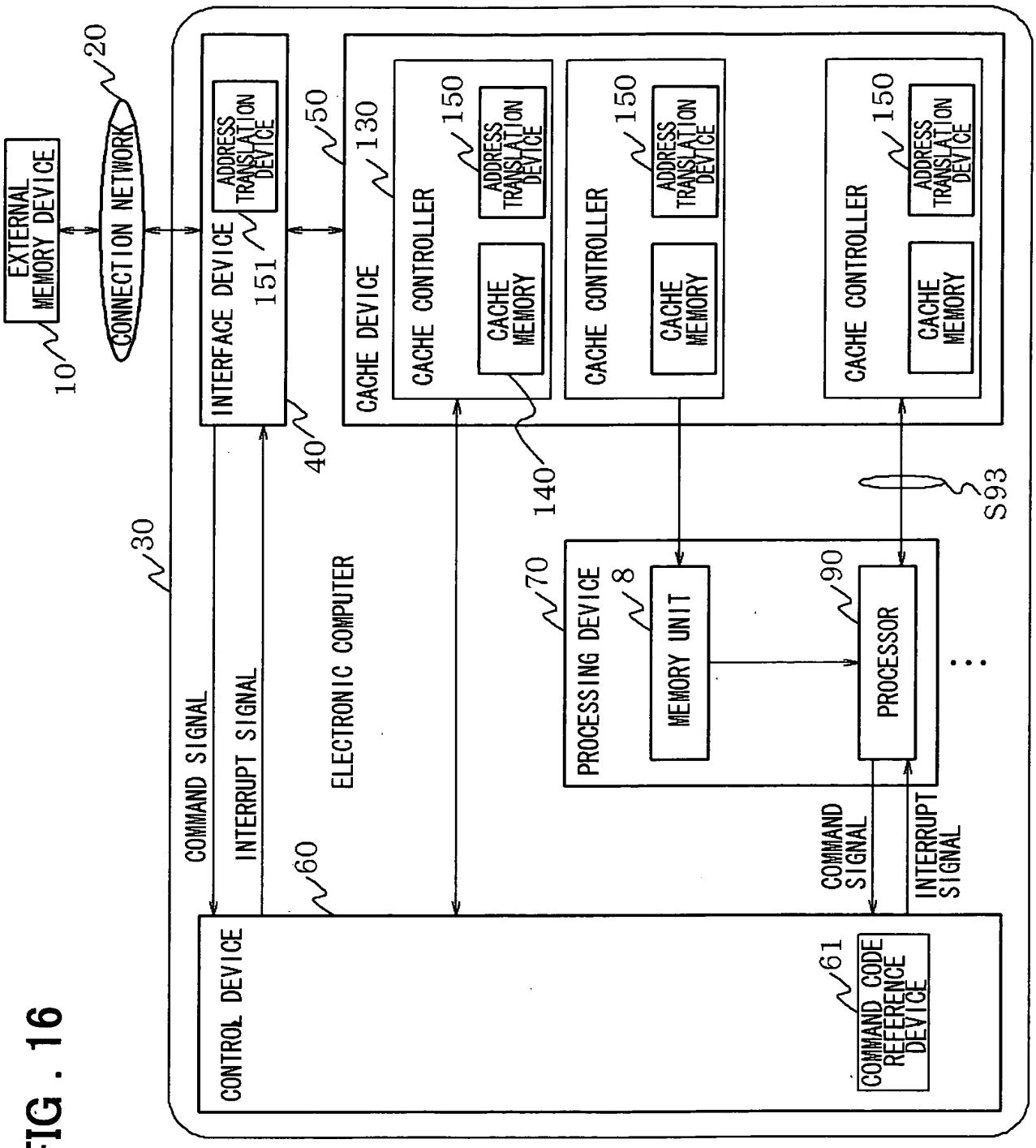
EXTERNAL MEMORY DEVICE
10
CONNECTION NETWORK
20
ELECTRONIC COMPUTER
30
INTERFACE DEVICE
ADDRESS TRANSLATION DEVICE
151
40
CACHE DEVICE
50
CACHE CONTROLLER
130
CACHE MEMORY
ADDRESS TRANSLATION DEVICE
150
140
S93
PROCESSING DEVICE
70
MEMORY UNIT
8
PROCESSOR
90
CONTROL DEVICE
60
COMMAND SIGNAL
INTERRUPT SIGNAL
COMMAND CODE REFERENCE DEVICE
61

FIG. 17

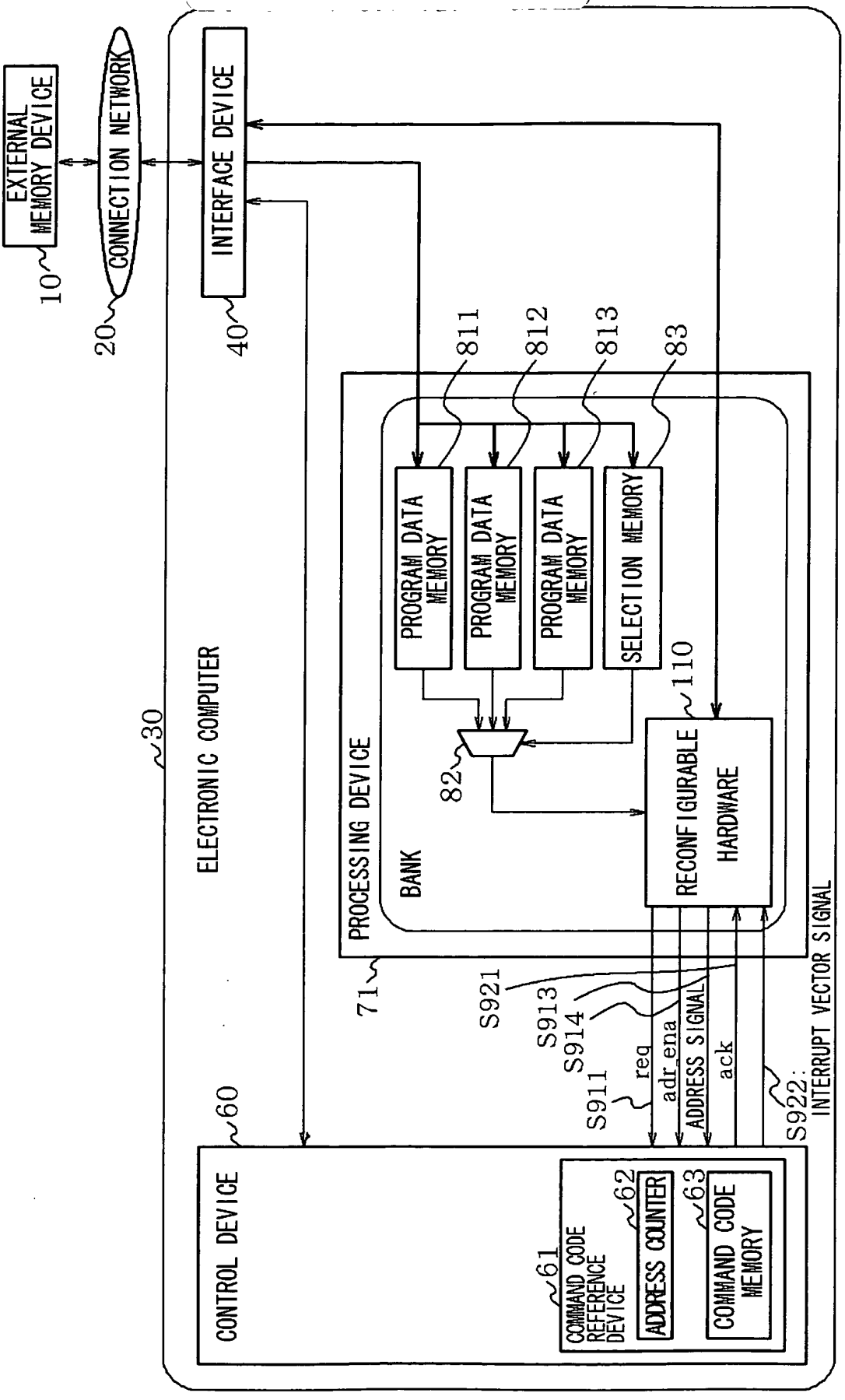
EXTERNAL MEMORY DEVICE
10
CONNECTION NETWORK
20
INTERFACE DEVICE
40
ELECTRONIC COMPUTER
30
811
812
813
83
PROGRAM DATA MEMORY
PROGRAM DATA MEMORY
PROGRAM DATA MEMORY
SELECTION MEMORY
110
82
RECONFIGURABLE HARDWARE
PROCESSING DEVICE
BANK
71
S921
S913
S914
S911
req
adr_ena
ADDRESS SIGNAL
ack
S922:
INTERRUPT VECTOR SIGNAL
CONTROL DEVICE
60
COMMAND CODE REFERENCE DEVICE
61
ADDRESS COUNTER
62
COMMAND CODE MEMORY
63

FIG . 18

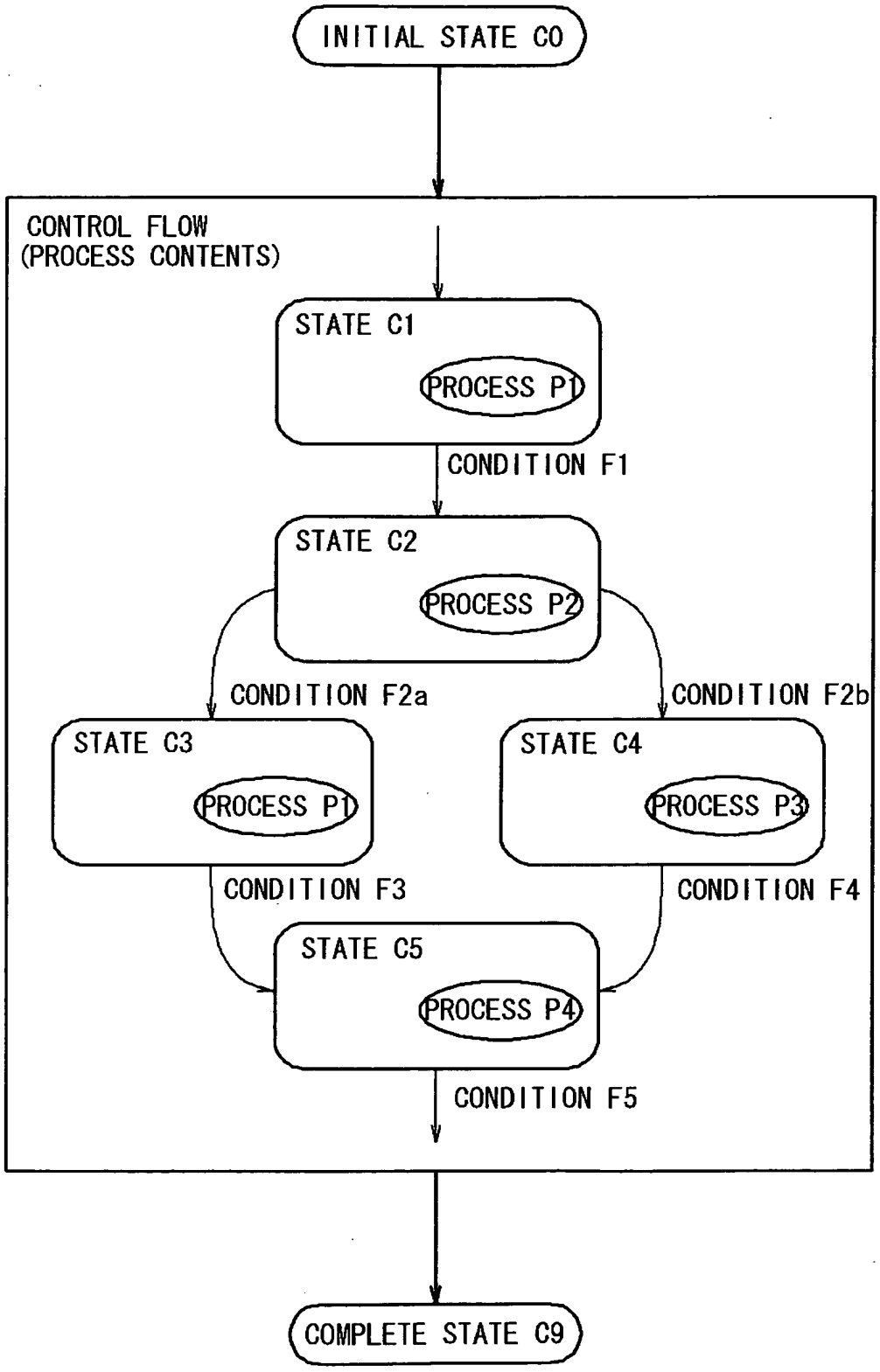
INITIAL STATE C0
CONTROL FLOW
(PROCESS CONTENTS)
STATE C1
PROCESS P1
CONDITION F1
STATE C2
PROCESS P2
CONDITION F2a
CONDITION F2b
STATE C3
PROCESS P1
STATE C4
PROCESS P3
CONDITION F3
CONDITION F4
STATE C5
PROCESS P4
CONDITION F5
COMPLETE STATE C9

FIG . 19

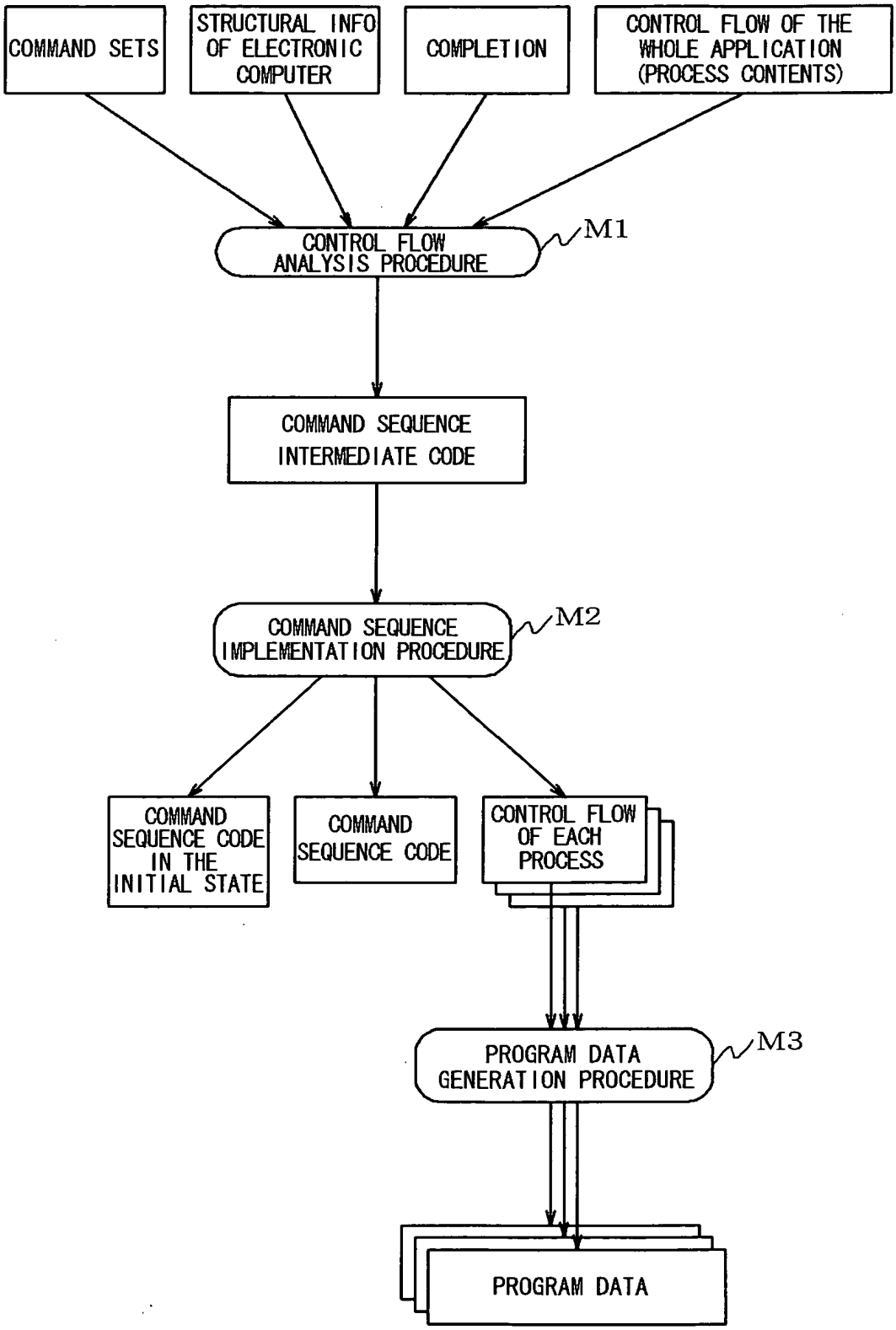
COMMAND SETS
STRUCTURAL INFO OF ELECTRONIC COMPUTER
COMPLETION
CONTROL FLOW OF THE WHOLE APPLICATION (PROCESS CONTENTS)
CONTROL FLOW ANALYSIS PROCEDURE
M1
COMMAND SEQUENCE INTERMEDIATE CODE
COMMAND SEQUENCE IMPLEMENTATION PROCEDURE
M2
COMMAND SEQUENCE CODE IN THE INITIAL STATE
COMMAND SEQUENCE CODE
CONTROL FLOW OF EACH PROCESS
PROGRAM DATA GENERATION PROCEDURE
M3
PROGRAM DATA

FIG . 20

PROCESS CONTENT	STATE	TRANSITION CONDITION	MOVES TO	PROGRAM DATA MEMORY USED	COMMAND SEQUENCE INTERMEDIATE CODE	
—	INITIAL STATE C0	—	STATE C1	811	load_prg 812, PM1 wait_prg 812, PM1 interrupt 71 , C1 activate 812 load_prg 813, PM2	SQ0
PROCESS P1	STATE C1	CONDITION F1 AND INTERRUPT VECTOR=C1	STATE C2	812	wait_prg 813, PM2 activate 813 load_prg 811, PM3	SQ1
	STATE C3	CONDITION F3 AND INTERRUPT VECTOR=C3	STATE C5		wait_prg 813, PM4 activate 813	SQ3
PROCESS P2	STATE C2	CONDITION F2a	STATE C3	813	cancel_prg 811, PM3 interrupt 71 , C3 activate 812 load_prg 813, PM4	SQ2a
		CONDITION F2b	STATE C4		wait_prg 811, PM3 activate 811 load_prg 813, PM4	SQ2b
PROCESS P3	STATE C4	CONDITION F4	STATE C5	811	wait_prg 813, PM4 activate 813	SQ4
PROCESS P4	STATE C5	CONDITION F5	COMPLETION STATE C9	813	halt 71	SQ5

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Inventor(s): Takeshi INUO
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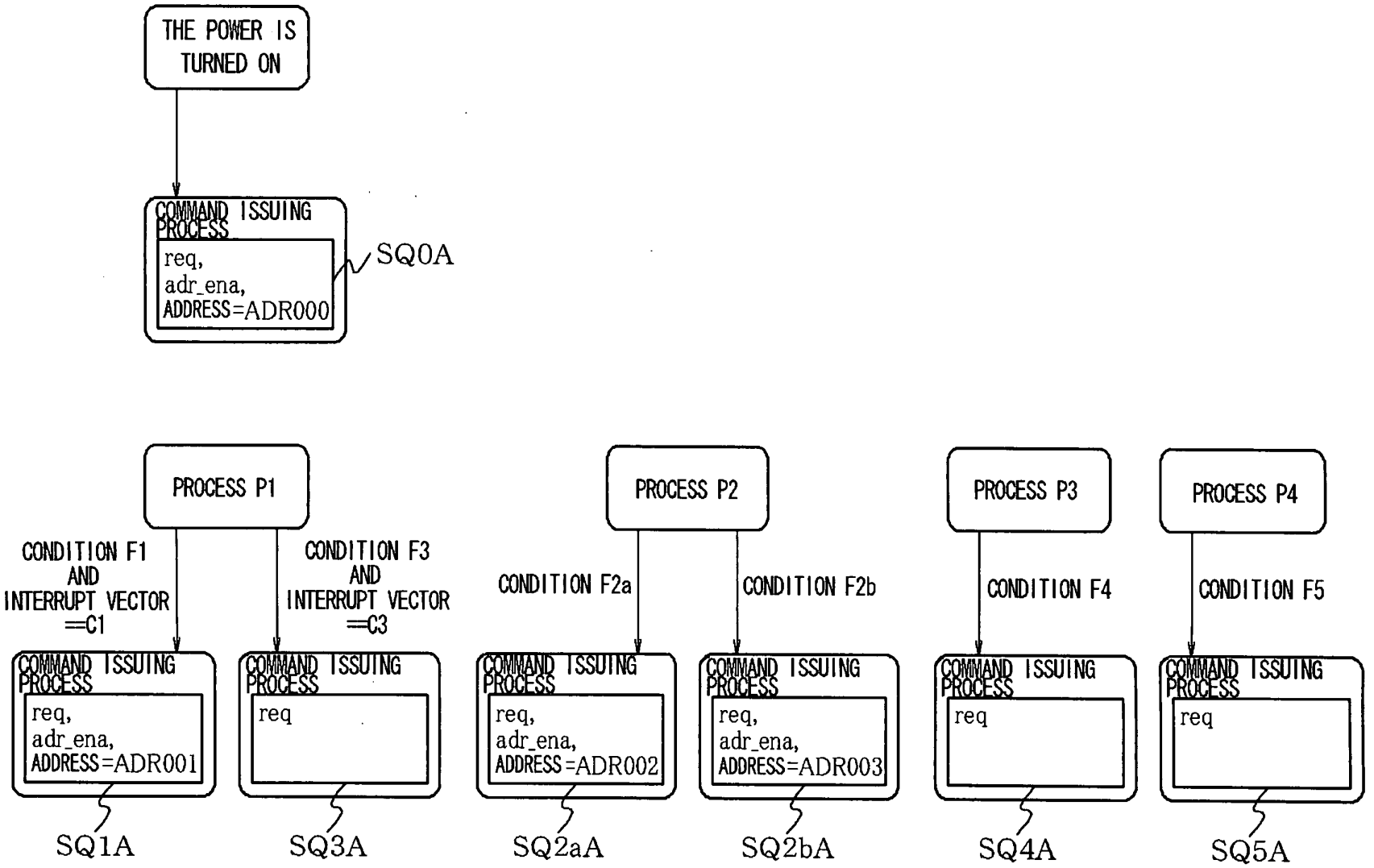
FIG . 21



Title: ELECTRONIC COMPUTER, SEMICONDUCTOR INTEGRATED CIRCUIT, CONTROL METHOD, PROGRAM GENERATION METHOD, AND PROGRAM
Inventor(s): Takeshi INUO
DOCKET NO.: 029471-0194

FIG . 22

BASE ADDRESS VALUE	OFFSET VALUE	COMMAND SEQUENCE			
		ADDRESS COUNTER CONTROL CODE		COMMAND CODE	
ADR000	+0	add_adr 1	cont	load_prg 812, PM1	SQ0
	+1	add_adr 1	cont	wait_prg 812, PM1	
	+2	add_adr 1	cont	interrupt 71 , C1	
	+3	add_adr 1	cont	activate 812	
	+4	add_adr 0	stop	load_prg 813, PM2	
ADR001	+0	add_adr 1	cont	wait_prg 813, PM2	SQ1
	+1	add_adr 1	cont	activate 813	
	+2	add_adr 0	stop	load_prg 811, PM3	
ADR002	+0	add_adr 1	cont	cancel_prg 811, PM3	SQ2a
	+1	add_adr 1	cont	interrupt 71 , C3	
	+2	add_adr 1	cont	activate 812	
	+3	load_adr ADR004	stop	load_prg 813, PM4	
ADR003	+0	add_adr 1	cont	wait_prg 811, PM3	SQ2b
	+1	add_adr 1	cont	activate 811	
	+2	load_adr ADR004	stop	load_prg 813, PM4	
ADR004	+0	add_adr 1	cont	wait_prg 813, PM4	SQ3,SQ4
	+1	add_adr 1	stop	activate 813	
	+2	add_adr 0	stop	halt 71	SQ5

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Inventor(s): Takeshi INUO
DOCKET NO.: 029471-0194

FIG . 23

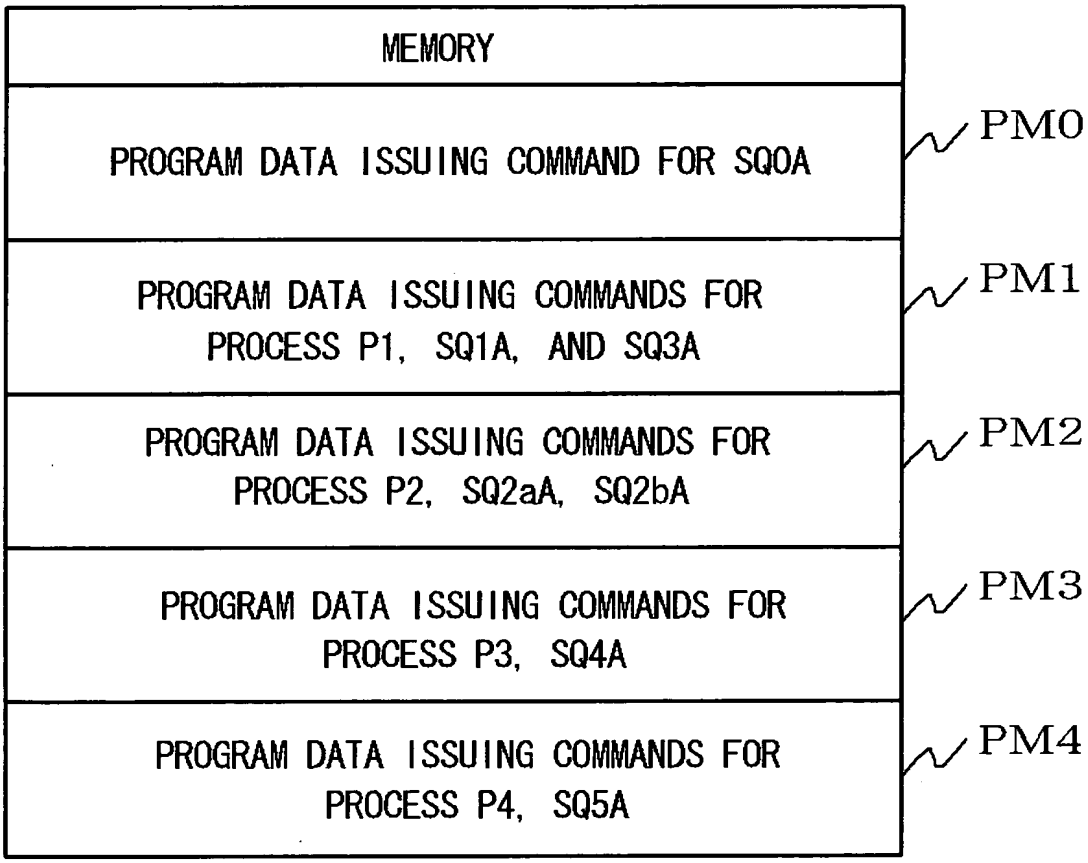
MEMORY
PROGRAM DATA ISSUING COMMAND FOR SQ0A
PM0
PROGRAM DATA ISSUING COMMANDS FOR PROCESS P1, SQ1A, AND SQ3A
PM1
PROGRAM DATA ISSUING COMMANDS FOR PROCESS P2, SQ2aA, SQ2bA
PM2
PROGRAM DATA ISSUING COMMANDS FOR PROCESS P3, SQ4A
PM3
PROGRAM DATA ISSUING COMMANDS FOR PROCESS P4, SQ5A
PM4

FIG . 24

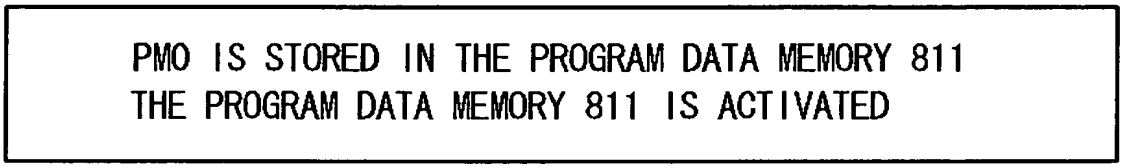
PMO IS STORED IN THE PROGRAM DATA MEMORY 811
THE PROGRAM DATA MEMORY 811 IS ACTIVATED

FIG. 25

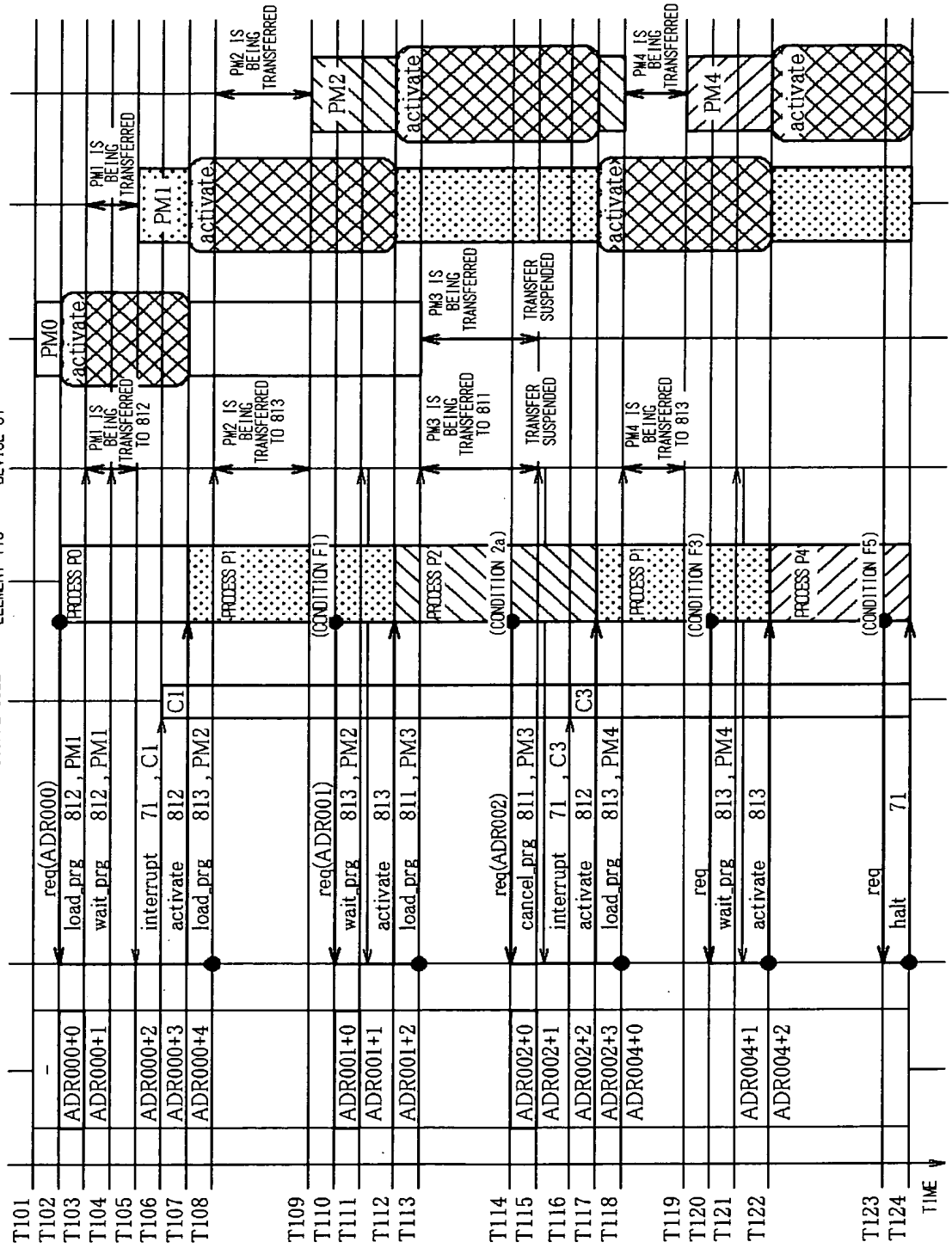
THE VALUE OF THE ADDRESS COUNTER 62
THE OPERATIONAL CONTENT OF THE CONTROL DEVICE 60
THE CONTENT OF THE INTERRUPT VECTOR SIGNAL S922
THE OPERATIONAL CONTENT OF THE PROCESSING ELEMENT 110
THE OPERATIONAL CONTENT OF THE PROGRAM DATA TRANSFER DEVICE 51
THE CONTENT HELD BY THE PROGRAM DATA MEMORY 811
THE CONTENT HELD BY THE PROGRAM DATA MEMORY 812
THE CONTENT HELD BY THE PROGRAM DATA MEMORY 813
TIME
T101
T102
T103
T104
T105
T106
T107
T108
T109
T110
T111
T112
T113
T114
T115
T116
T117
T118
T119
T120
T121
T122
T123
T124
ADR000+0
ADR000+1
ADR000+2
ADR000+3
ADR000+4
ADR001+0
ADR001+1
ADR001+2
ADR002+0
ADR002+1
ADR002+2
ADR002+3
ADR004+0
ADR004+1
ADR004+2
req(ADR000)
load_prg 812 , PM1
wait_prg 812 , PM1
interrupt 71 , C1
activate 812
load_prg 813 , PM2
req(ADR001)
wait_prg 813 , PM2
activate 813
load_prg 811 , PM3
req(ADR002)
cancel_prg 811 , PM3
interrupt 71 , C3
activate 812
load_prg 813 , PM4
req
wait_prg 813 , PM4
activate 813
req
halt 71
C1
C3
PROCESS P0
PROCESS P1
(CONDITION F1)
PROCESS P2
(CONDITION 2a)
PROCESS P1
(CONDITION F3)
PROCESS P4
(CONDITION F5)
PM1 IS BEING TRANSFERRED TO 812
PM2 IS BEING TRANSFERRED TO 813
PM3 IS BEING TRANSFERRED TO 811
PM4 IS BEING TRANSFERRED TO 813
TRANSFER SUSPENDED
TRANSFER SUSPENDED
PM0
activate
PM1 IS BEING TRANSFERRED
PM1
activate
PM2 IS BEING TRANSFERRED
PM2
activate
PM3 IS BEING TRANSFERRED
activate
PM4 IS BEING TRANSFERRED
PM4
activate

FIG. 26

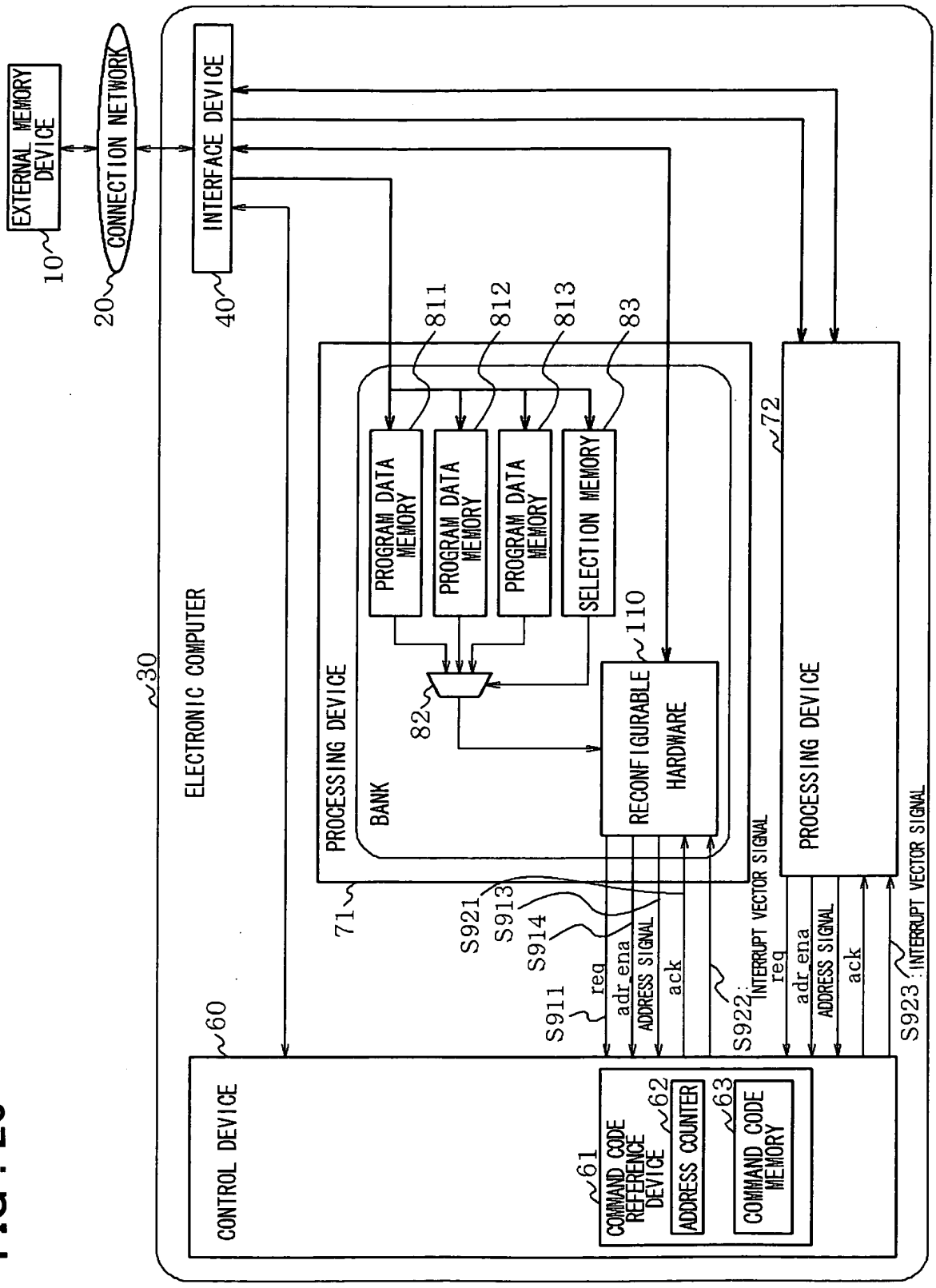
EXTERNAL MEMORY DEVICE
10
CONNECTION NETWORK
20
INTERFACE DEVICE
40
ELECTRONIC COMPUTER
30
811
812
813
83
PROGRAM DATA MEMORY
PROGRAM DATA MEMORY
PROGRAM DATA MEMORY
SELECTION MEMORY
82
110
RECONFIGURABLE HARDWARE
PROCESSING DEVICE
BANK
71
72
PROCESSING DEVICE
S921
S913
S914
S911
req
adr ena
ADDRESS SIGNAL
ack
INTERRUPT VECTOR SIGNAL
S922
S923
CONTROL DEVICE
60
COMMAND CODE REFERENCE DEVICE
61
ADDRESS COUNTER
62
COMMAND CODE MEMORY
63

FIG . 27

BASE ADDRESS VALUE	OFFSET VALUE	COMMAND SEQUENCE			
		ADDRESS COUNTER CONTROL CODE		COMMAND CODE	
ADR000	+0	add_adr 1	cont	load_prg 812, PM1	SQ0
	+1	add_adr 1	cont	wait_prg 812, PM1	
	+2	add_adr 1	cont	interrupt 71 , C1	
	+3	add_adr 1	cont	activate 812	
	+4	add_adr 0	stop	load_prg 813, PM2	
ADR001	+0	add_adr 1	cont	wait_prg 813, PM2	SQ1
	+1	add_adr 1	cont	activate 813	
	+2	add_adr 0	stop	load_prg 811, PM3	
ADR002	+0	add_adr 1	cont	cancel_prg 811, PM3	SQ2a
	+1	add_adr 1	cont	interrupt 71 , C3	
	+2	add_adr 1	cont	activate 812	
	+3	load_adr ADR004	stop	load_prg 813, PM4	
ADR003	+0	add_adr 1	cont	wait_prg 811, PM3	SQ2b
	+1	add_adr 1	cont	activate 811	
	+2	load_adr ADR004	stop	load_prg 813, PM4	
ADR004	+0	add_adr 1	cont	wait_prg 813, PM4	SQ3,SQ4
	+1	add_adr 1	stop	activate 813	
	+2	add_adr 1	cont	halt 71	SQ5B
	+3	add_adr 0	stop	interrupt 72,END71	

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Inventor(s): Takeshi INUO
DOCKET NO.: 029471-0194

FIG . 28

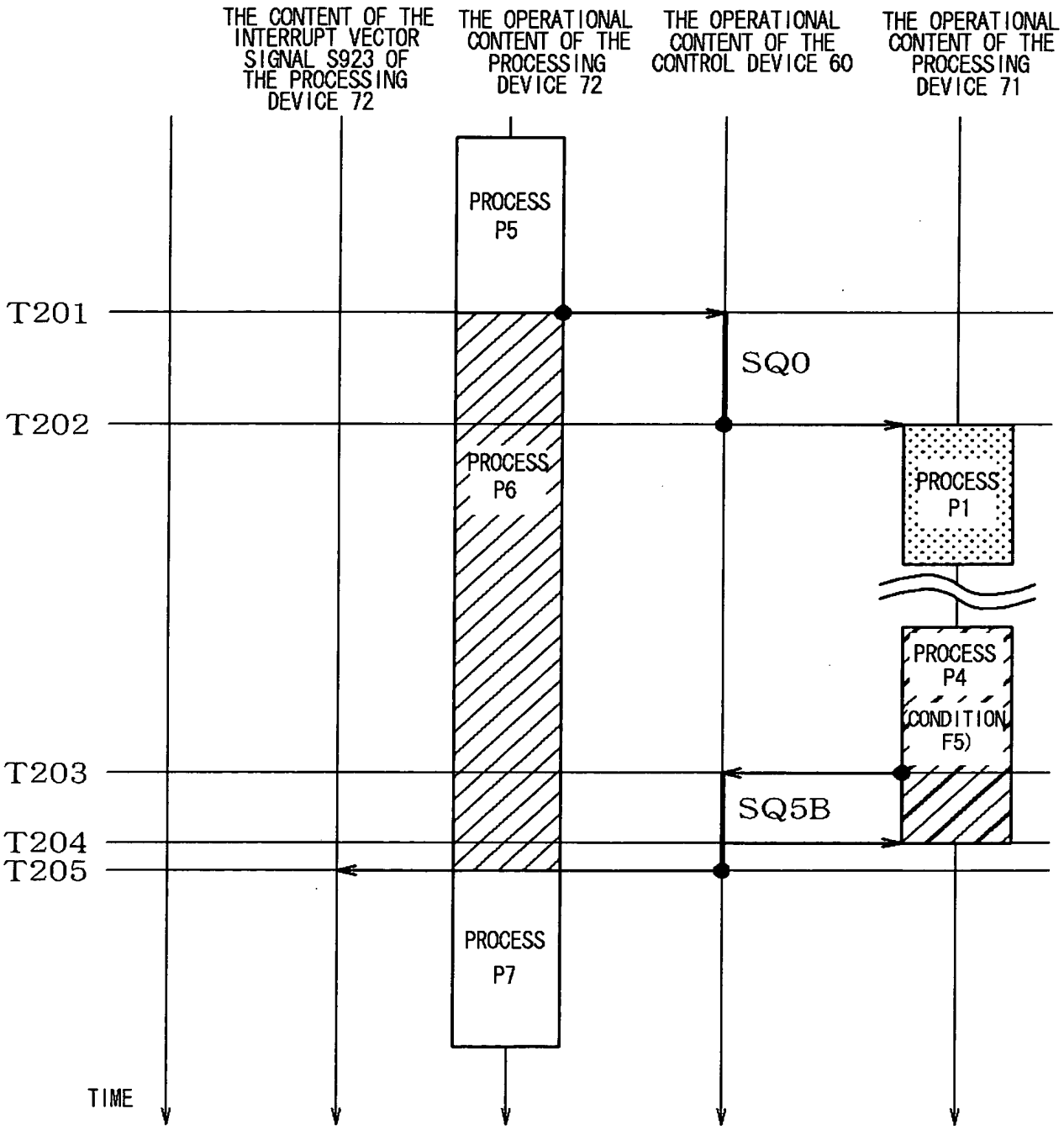
THE CONTENT OF THE INTERRUPT VECTOR SIGNAL S923 OF THE PROCESSING DEVICE 72
THE OPERATIONAL CONTENT OF THE PROCESSING DEVICE 72
THE OPERATIONAL CONTENT OF THE CONTROL DEVICE 60
THE OPERATIONAL CONTENT OF THE PROCESSING DEVICE 71
PROCESS P5
T201
SQ0
T202
PROCESS P6
PROCESS P1
PROCESS P4
CONDITION F5)
T203
SQ5B
T204
T205
PROCESS P7
TIME

FIG . 29

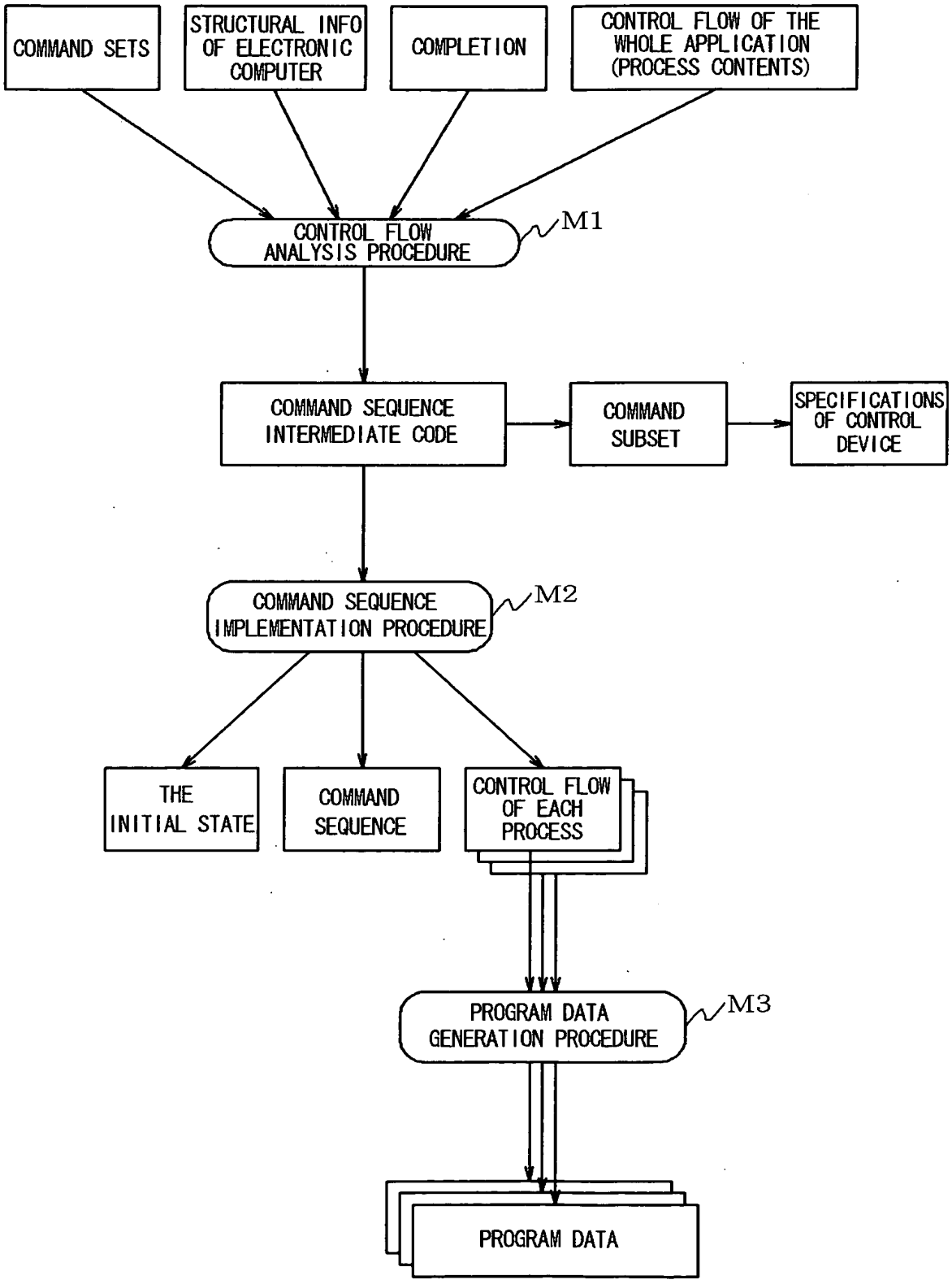
COMMAND SETS
STRUCTURAL INFO OF ELECTRONIC COMPUTER
COMPLETION
CONTROL FLOW OF THE WHOLE APPLICATION (PROCESS CONTENTS)
CONTROL FLOW ANALYSIS PROCEDURE
M1
COMMAND SEQUENCE INTERMEDIATE CODE
COMMAND SUBSET
SPECIFICATIONS OF CONTROL DEVICE
COMMAND SEQUENCE IMPLEMENTATION PROCEDURE
M2
THE INITIAL STATE
COMMAND SEQUENCE
CONTROL FLOW OF EACH PROCESS
PROGRAM DATA GENERATION PROCEDURE
M3
PROGRAM DATA

FIG . 30 PRIOR ART

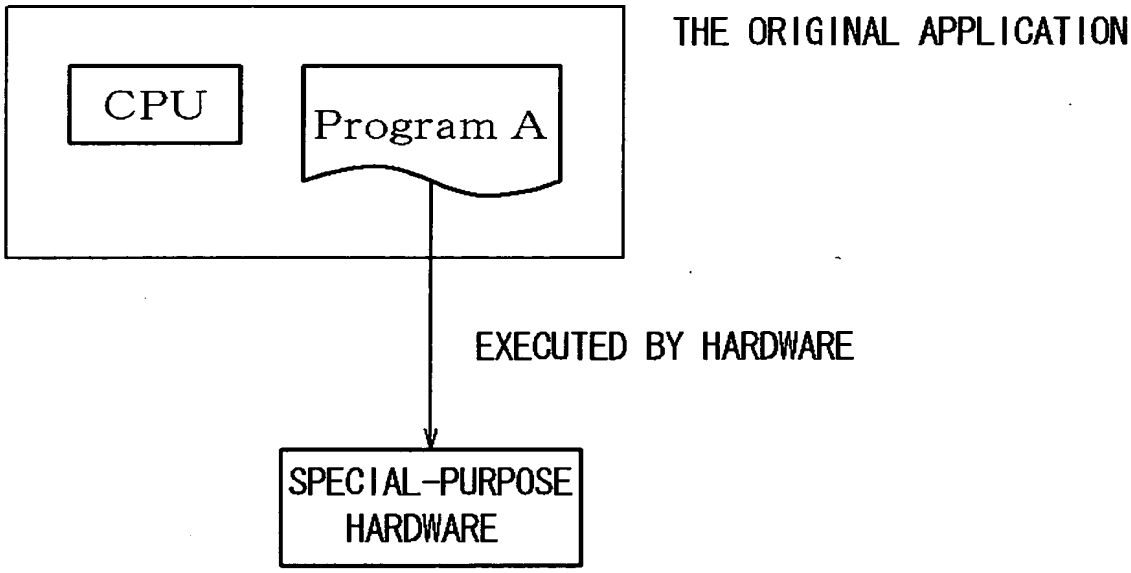

FIG . 31

PRIOR ART

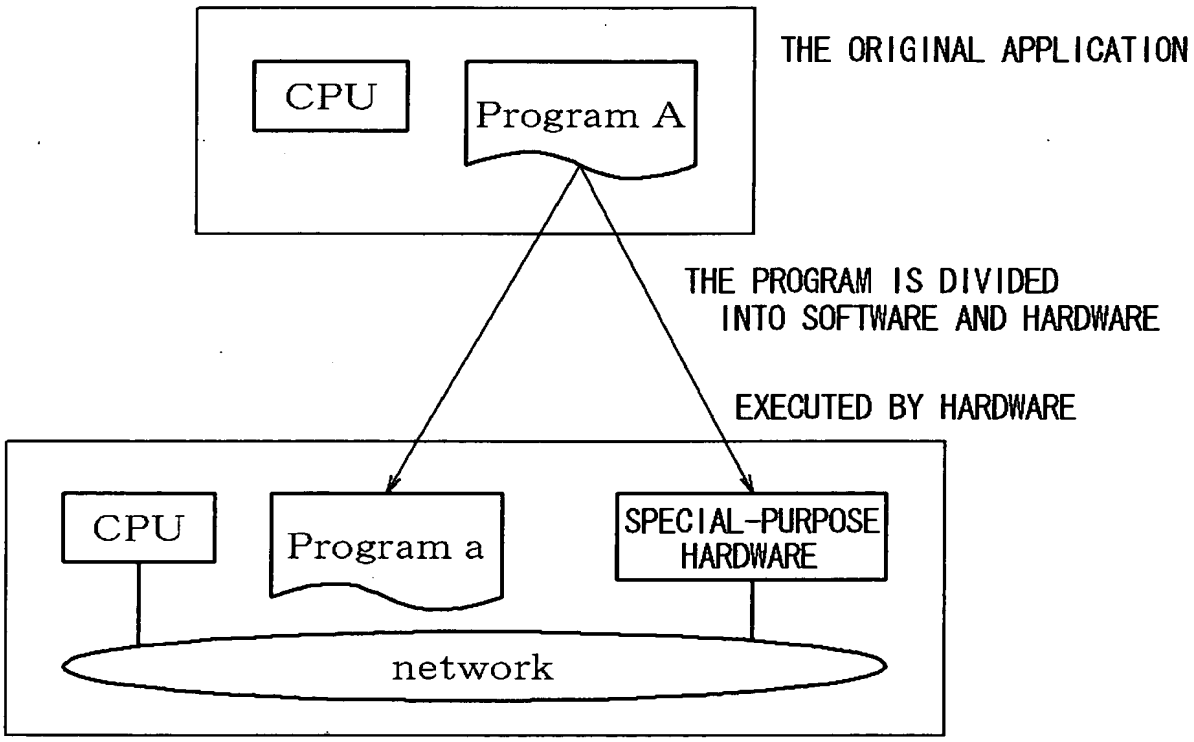

FIG . 32

PRIOR ART